MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

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Summary

This contract seeks to develop a family of thin-film stimulating arrays for use in neural prostheses. STIM-2B/-3B are two- and three-dimensional arrays of stimulating sites on 400µm centers. The probes have four channels and 64-sites. Any selected site can be used for either recording or stimulation. Current generation is off-chip. The high-end probes STIM-2/-3 are similar except they use on-chip current generation via 8-bit digital to analog converters.

During the last quarter, the microassembly station used for the creation of multi-probe three-dimensional electrode arrays has been improved and used for the realization of a number of fully-functional units. The external electronics needed to interface with these arrays has been completed and is functional at frequencies of up to 9.5Mb/sec. Work has also gone forward on the redesign of STIM-2. Most of the probe redesign has been completed, including a dedicated recording line and multi-level anodic bias option. A switched-capacitor digital-to-analog converter (DAC) has been explored for possible use in current generation, but in spite of advantages in power and accuracy is probably less attractive than the transistor/resistive DACs due to problems with leakage from the storage nodes and the problems of doing a high-quality sample-and-hold function on-chip. DAC circuits capable of operating from a single supply voltage have also been explored. These offer considerable circuit simplifications over dual-supply circuits but depend on electrical isolation between the probe and the tissue, which is not possible using active probes. The degree to which the conducting substrate may distort the current fields in such an arrangement is not precisely known but will be investigated. In the meantime, dual-supply operation will continue. Single- and dual-supply circuits for a platform-mounted telemetry system have been designed and are now in fabrication. The circuits include voltage regulator, power-on reset, clock recovery, and data detector blocks. We expect to complete the design of STIM-2 during the coming term and to test the telemetry circuit blocks in preparation for a fully wireless active recording system.

MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

1. Introduction

The goal of this contract is the development of active multi-channel arrays of stimulating electrodes suitable for studies of neural information processing at the cellular level and for a variety of closed-loop neural prostheses. The probes should be able to enter neural tissue with minimal disturbance to the neural networks there and deliver highly-controlled (spatially and temporally) charge waveforms to the tissue on a chronic basis. The probes consist of several thin-film conductors supported on a micromachined silicon substrate and insulated from it and from the surrounding electrolyte by silicon dioxide and silicon nitride dielectric films. The stimulating sites are activated iridium, defined photolithographically using a lift-off process. Passive probes having a variety of site sizes and shank configurations have been fabricated successfully in past contracts and have been distributed to a number of research organizations nationally for evaluation in many different research preparations. For chronic use, the biggest problem associated with these passive stimulating probes concerns their leads, which must interface the probe to the outside world. Even using silicon-substrate ribbon cables, the number of allowable interconnects is necessarily limited, and yet a great many stimulating sites are ultimately desirable in order to achieve high spatial localization of the stimulus currents.

The integration of signal processing electronics on the rear of the probe substrate (creating an "active" probe) allows the use of serial digital input data which can be de-multiplexed on the probe to provide access to a large number of stimulating sites from a very few leads. Our goal in this area is to develop a family of active probes capable of chronic implantation in tissue. For such probes, the digital input data must be translated on the probe into per-channel current amplitudes that are then applied to tissue through the sites. Such probes generally require five external leads, virtually independent of the number of sites used. As discussed in previous reports, we have designed a series of active probes containing CMOS signal processing electronics. Two of these probes have been completed and are designated as STIM-1A and STIM-1B. A third probe, STIM-2, is now beginning a final iteration and is a second-generation version of our original high-end first-generation design, STIM-1. All three probes provide 8-bit resolution in digitally setting the per-channel current amplitudes. STIM-1A and -1B offer a biphasic range using ±5V supplies from 0μA to ±254μA with a resolution of 2μA, while STIM-2 has a range from 0 to ±127μA with a resolution of 1μA. STIM-2 offers the ability to select 8 of 64 electrode sites and to drive these sites independently and in parallel, while STIM-1A allows only 2 of 16 sites to be active at a time (bipolar operation). STIM-IB is a monopolar probe, which allows the user to guide an externally-provided current to any one of 16 sites as selected by the digital input address. The high-end STIM-2 contains provisions for numerous safety checks and for features such as remote impedance testing in addition to its normal operating modes. It also offers the option of being able to record from any one of the selected sites in addition to stimulation. It will be the backbone of a

multi-probe three-dimensional (3D) 1024-site array (STIM-3) now in development. A new probe, STIM-2B, has recently been added to this set. It offers 64-site capability with off-chip generation of the stimulus currents for four separate channels. These channels are organized in four groups so that each current can be directed to any of the 16 sites in its group. Each selected channel can be programmed for either stimulation or recording. On-chip recording amplifiers offer a gain of 50; alternatively, the neural activity can be recorded using off-chip amplifiers interfaced through the normal stimulating channels. This probe is available in both 2D and 3D versions (as STIM-2B/3B) and is now being used in-vivo.

During the past quarter, we have continued to fabricate passive probe structures for a variety of users. We have improved our microassembly station and used it to create arrays of active probes (STIM-3B). We have also packaged the external interface hardware required for such arrays and are now ready for their in-vivo use. Additional circuits have been explored for use on STIM-2, including a switched-capacitor DAC and circuits capable of running from a single supply. Circuits for a telemetry interface for the active probes have been designed and are now being fabricated. The results in each of these areas are described more fully in the sections below.

2. Active Stimulating Probe Development

Recent activities in active stimulating probe development have focused on the 3D array assembly process and the subsequent bonding of the 90^{o} gold beam leads. The assembly equipment has been updated and beam-lead bonding has been successfully performed. We have also completed packaging of the external user interface hardware, which should help reduce noise problems and protect the circuitry during use.

STIM-2B/3B

STIM-2B is a second-generation probe, a version of our simplest active stimulating probe, STIM-1B. It is a four-channel, 16-shank, 64-site probe which routes four externally generated stimulus signals to 1-of-16 sites per channel. The logical extension of STIM-2B is to make it into a 3-dimensional (3D) array, which is exactly what we did to realize STIM-3B. STIM-3B is set up in a platform configuration with an integrated ribbon cable for connection to a percutaneous plug, allowing use of the device in chronic experiments. The differences between STIM-2B and –3B are some structural modifications to allow connection to a 3D-platform assembly and a few additional circuit blocks to facilitate the addressing of multiple probes in a 3D array.

The STIM-2B/3B probes are expected to provide an important tool for performing some very important and interesting experiments by allowing the acute and chronic stimulation access to a relatively large volume of neural tissue without mechanically repositioning of the probe. This capability is realized by utilizing a 20b shift register to load four 4b site addresses which are decoded by a 1-of-16 nand-type decoder to connect the desired site to an analog input/output pad through a large CMOS passgate transistor

thereby allowing the 'steering' of externally generated currents to the addressed site. A recording function is included and is addressed by a fifth bit included with the 4b site address. This fifth bit selects between stimulation mode and recording mode by selecting either a direct path to the I/O pad from the site or a path through an amplifier for recording from the same site. Each I/O channel has its own dedicated amplifier so that the functionality of all of the channels is independent of each other except for the up-front data input circuitry.

In order to allow addressing of multiple probes in a 3D array, STIM-3B has an extra 4b serial input shift-register which, when the bits are set, connects the corresponding I/O channel of the probe onto a common I/O bus on the platform. All of the extra registers of the probes in a STIM-3B array are connected in series via platform leads to form an extended or virtual register. The virtual register enables all of the probes of a 3D array to be addressed with only two address lines, a channel enable address line and a site address line. This architecture does have a limitation in that it doe not allow independent use of the same site address on two separate probes in the array. The slightly reduced flexibility was considered a reasonable sacrifice to achieve a reduction in circuit complexity and more importantly lead count.

Rather than waste area on the active CMOS probe mask set, the 3D structural pieces were designed on a completely separate mask set which only required six masks and was essentially the same fabrication process as is used for passive probes. The only difference is that instead of site and pad masks, there is a single beam/pad electroplating mask. The electroplating mask is used as the final step to form the 5µ-thick gold beam lead interconnects and pads on the platforms after the field etch has been done.

Following fabrication and etch-out of all of the different components of the 3D arrays, the arrays must be assembled and the 90^{o} gold beam lead interconnects must be bonded in order for the input/output signals to be able to pass between the platform and the individual probes. Assembly of the 3D arrays is not an easy task to perform considering that all 16 tips of the 15µ-thick probe shanks must be threaded into the appropriate 19µ-wide slit in the platform. In the past, this task was made even more difficult by the somewhat flimsy micro-manipulator that was being used. Simply touching one of the manipulator adjustment micrometers was enough to cause the probe holder to move significantly due to flexing of the mechanism. The probe placement manipulator has been replaced by a much more rigid manipulator, as shown in Fig. 1, which does not have this problem. The new manipulator has improved the assembly process significantly though it is still not an easy task. We are continually looking for means of improving this task since it is still fairly labor intensive. When these 3D arrays begin to be made in large quantities, this step will have to become much faster and easier. We are considering the possibility of using micromachined jigs to aid in guiding the probes into place in the array platforms.

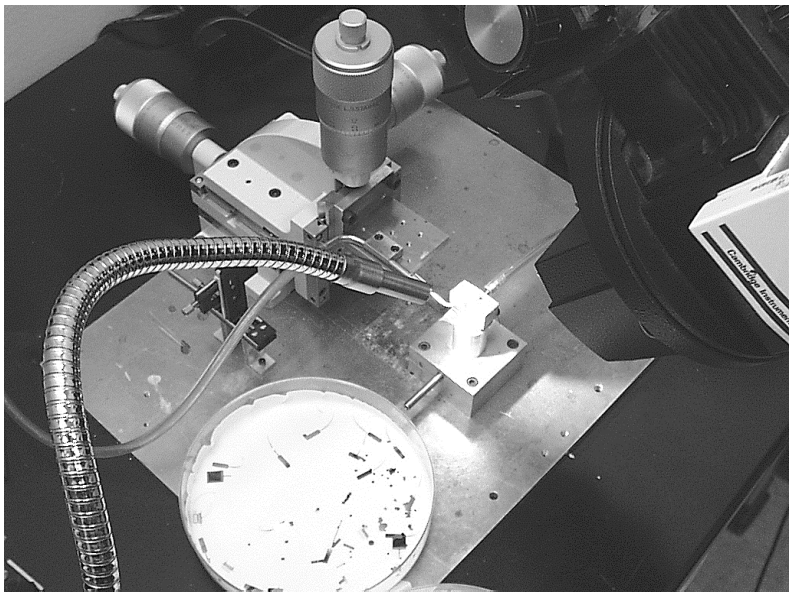

Fig. 1: The updated 3D probe array assembly system including the more rigid manipulator for probe placement. Included in the lower left is a dish of the 3D platforms and the associated structural pieces ready for assembly.

Once the arrays are assembled, the gold beam leads on the probes must be bonded to the corresponding pad on the platform. This is a challenging task as well because of the small separation between rows of beam leads on adjacent probes. The beam leads used on the STIM-3B probes were actually split into two 40µm wide smaller beams with a 10µm gap between them and a 60µm space to the next double beam lead. The corresponding pads on the platform are 110µm wide with a 40µm spacing between adjacent pads. The beam leads were originally split because it was felt that this would increase the likelihood of one of the beams surviving should there be damage to the other for whatever reason during fabrication and release. As it turns out, this was probably not necessary since these beams emerge from the fabrication and bonding process with very high yield.

By using a very narrow ultrasonic bonding wedge, we have been able to successfully bond the beam leads to the platform pads, as shown in Fig. 2, without damaging the probe outriggers. One of the remaining critical dimensions is the distance that the first beam lead must be from the main part of the probe back-end in order for the bonding wedge to clear the probe area when making the bond. If the first beam lead is too close to the probe body, the bonding wedge will damage the probe or spacer when coming down to make the bond. A very conservative distance was allowed in the current design; thus, it was not a problem. We are considering the possibility of a specially designed bonding wedge which would make it possible to bond right up to the edge of the probe back-end by having the contacting surface at the back-edge of the wedge instead of the front-edge. In future 3D array designs, it will be important to begin to shrink these dimensions in order to reduce the overall array size. It may also be

possible to eliminate the second beam lead of the split pair, thus reducing the interconnect area by almost a factor of two.

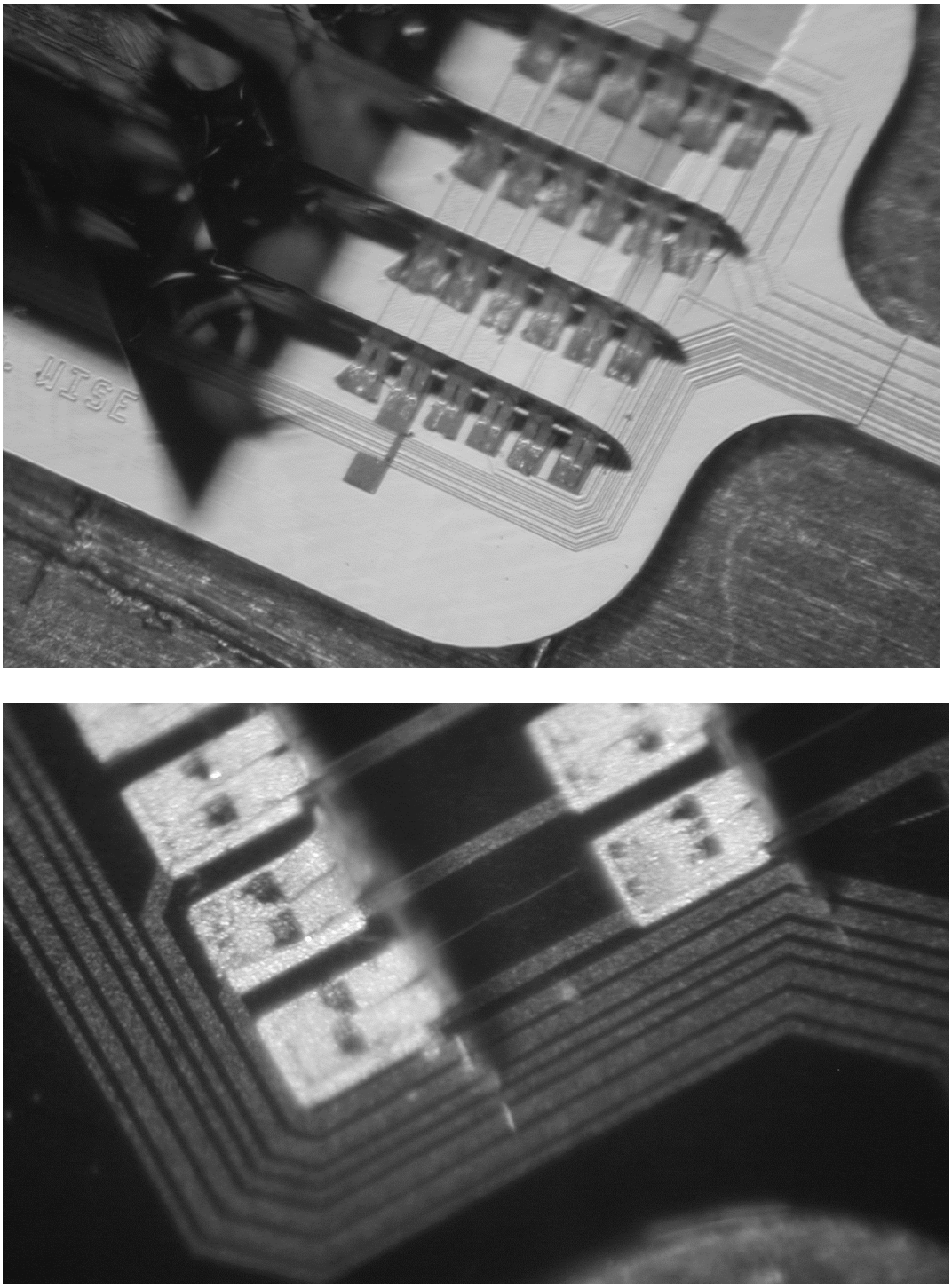

Fig. 2: The ultrasonically bonded gold beam leads for making the 90^{o} probe-to-platform interconnect of an assembled 3D STIM-3B probe array.

External Stimulating Interface System

We have designed and constructed an interface system for active stimulating probes, as described and shown in previous reports. The printed circuit board realization of our hardware design, which is referred to as REMSTIM, has been fabricated and tested. This version of the system operates much faster and supports a probe bit rate up to 9.5Mbits/sec and down to a division by 256. The system is operated remotely via a serial cable link to a personal computer. Graphical software has been developed for easy use of the system and a command-line interpreter is included in a separate window that allows for fine-grain control over the remote system. Whereas the graphical component of the interface is intended as an easy-to-use method for performing common functions, the command-line interpreter can be used to effect any other function not supported by the graphical interface.

A small probe connector PCB was designed and fabricated for the purpose of providing a platform on which to mount the probe stalks as well as to hold circuitry for such things as the high output resistance current sources for the STIM-2B/3B probes, probe power supply monitoring circuits, and recording buffers. As reported in previous progress reports, the circuits on this board have been shown to perform very well in bench testing. The PCB in its current form was fabricated entirely in-house; thus, it is somewhat larger than it might be if it were fabricated through an outside vendor. Fabrication of the board in-house limits the PCB to two layers of copper, while fabrication through an outside vendor would allow many more interconnect layers, thereby reducing the overall size to as little as half of its current size. The noise performance may also improve with the use of shielding plane layers in the board. Once we know that this design works well in *in-vivo* experiments, we may make additional boards through commercial PCB facilities in order to make the board much smaller and more easily used in *in-vivo* stimulation and/or recording preparations. Reduction in the size of the head-stage makes it easier to perform experiments by improving visibility during animal prep and probe insertion.

The external system has seen a number of improvements during the past quarter. Most of the improvements have had some cosmetic value, but the primary improvement is realized in signal noise reduction, physical protection, and ease of signal handling, both to and from the probe being operated. As is well known by those working in neural recording, minimization of noise from 60 cycle power or any other extraneous sources is absolutely essential for low-noise single-unit neural recordings. While most recordings are done in shielded recording booths, any lead that must travel into the booth (such as from the external interface system) has the potential of transmitting noise into the shielded area. For this reason, the external system should be well shielded to minimize the amount of noise that is carried into the booth from the external personal computer and DSP-board-related hardware. If the system is to be used for any type of simple neural recording, which it is capable of, noise control becomes even more critical.

The cable-termination/probe-connector (head-stage) board must first be protected from any contamination during experiments. Because of the very high output impedance

targeted for the current sources, any contamination on the circuit area of the board could result in significant low-resistance leakage paths, which would adversely affect performance. Thus, it was very important to mechanically protect the board. To this end, an aluminum case was machined just large enough to fit around the board, as can be seen in Figs. 3 and 4. A DIP socket for mounting the probe PCB stalk extends out from the end of the case and this is the only area of the board that is exposed during normal use. In order to provide protection to the leads, the exposed area of the PCB is coated with a sprayed-on high impedance conformal protective coating designed specifically for PCBs. Using aluminum for the protective case has the added benefit of allowing it to be grounded and used as a noise shield. With a shielded head-stage, a shielded cable, and a shielded REMSTIM board, the entire system is shielded right up to the probe.

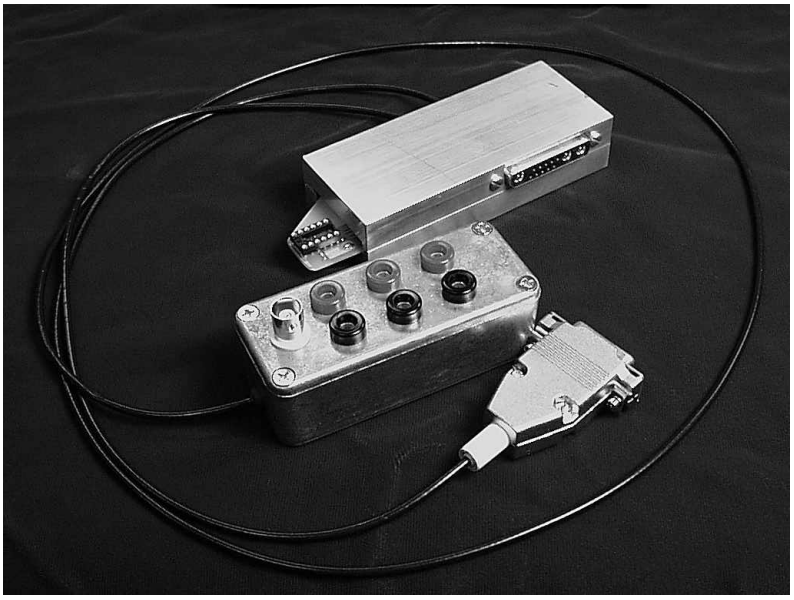

Fig. 3: The completed head-stage system with recording preamplifier connector and power supply current monitors and high speed data-out connection.

Two additional cables exit the head-stage casing. The first cable is terminated in a DB-15 connector, which connects directly into the existing recording preamplifiers located in the recording booth. This cable carries out the unity-gain buffered signal from the current source output/recording input node. Because of the design, the voltage at the current-source-output/recording-input node can be monitored with essentially no current loss during stimulation and minimal loading effects during the recording of neural signals. This capability is anticipated to be a very valuable tool in many different types of experiments.

The second cable is terminated in a break-out box. The break-out box has three pairs of banana plug receptacles, which allow the monitoring of several probe signals of interest. First, by measuring the difference between each pair, the power supply current for each of the power supplies to the probe can be monitored (I(V+), I(V-), I(Gnd)); thus,

a probe failure due to current leakage can be detected. Also, the absolute voltage that is actually being delivered to the probe can be monitored. A single BNC connector brings out the digital X-DATA signal returned from the STIM-3B X-DATA OUT connection, which can be observed and used for error checking.

The REMSTIM board has a significant amount of digital signals and therefore generates a large amount of noise. Since there are connections from this board to the probe connector board, it is almost impossible to completely eliminate all noise transmission into the vicinity of the probe; however, the amount of noise can be minimized. For this purpose, a metal case was used as the enclosure for the REMSTIM board. By grounding the case, any additional noise that might feed through from the external system can be minimized. The REMSTIM enclosure box is shown in Fig. 5.

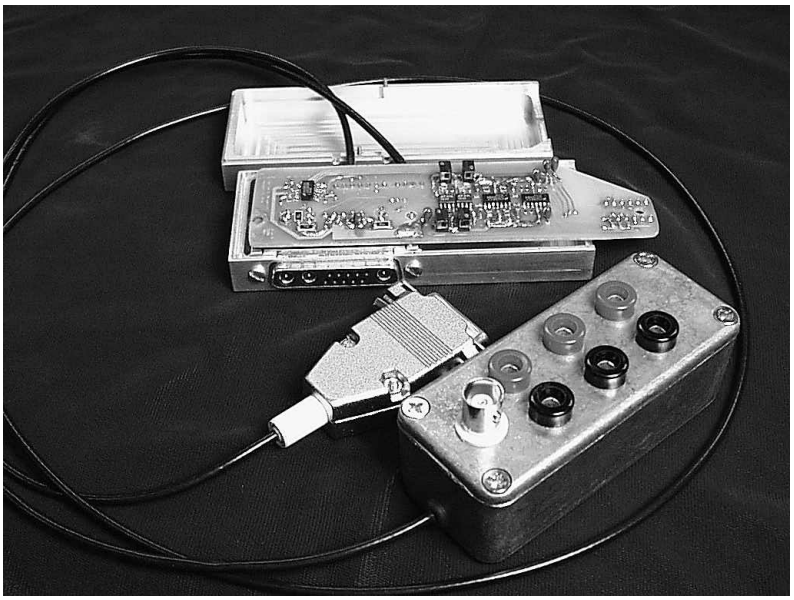

Fig. 4: The completed head-stage system with shielding case opened to reveal the cable-terminator/probe-connector board.

We are currently working on assembling completely functional 3D arrays, which we plan to use first in some *in-vitro* testing and then assuming satisfactory performance in *in-vivo* experiments. While assembling the arrays, we hope to develop a knowledge base that will enable us to make improvements in the assembly process in order to make it faster and safer for the devices. We are also in the process of making changes to the probe layouts to include probes with fewer, but longer, shanks, thereby maintaining the 64 sites/probe while accessing more depth and less width in tissue.

In the coming quarter, we plan to complete the collection of long-term *in-vitro* pulse testing data. We also plan to perform several experiments in-vivo with both the 2D and 3D arrays. In order to perform multiple-probe experiments, we will need to fabricate at least one more head-stage board, which we also plan to do early in the coming quarter.

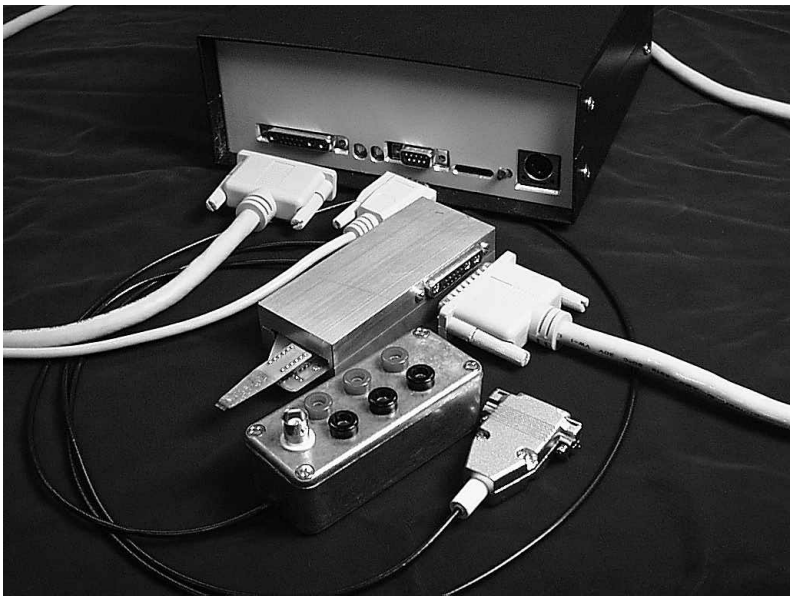

Fig. 5: The complete external system including the REMSTIM board enclosed in a metal shielding case, the associated cables and a STIM-2B probe mounted in the DIP socket.

3. Final Design of STIM-2

During the past three months, simulation and layout of the modified STIM-2 have been carried out to implement the new contract specifications. These include a dedicated data line for recording and multi-level anodic bias capability between pulses. In addition to these added features, we have continued to examine DAC designs to ensure the best possible operation from the redesigned probe. A resistor-weighted voltage DAC prototype was presented in the last quarterly report and is the leading contender for the generation of the stimulating currents; however, a monolithic capacitor-weighted DAC has also been considered for this function and for establishing the anodic bias level. Figure 6 shows the schematic of a 3-bit switched-capacitor voltage converter. At the start of conversion all capacitors are discharged; they are then connected to the relative reference voltage source corresponding to the input D0 to establish the precharge condition. When conversion starts, every capacitor, depending on the input bit information D1~D3, is either connected to ground or remains in the reference position; thus, binary weighting is obtained by the charge redistribution. Figures 7 and 8 show the DAC performance in both polarities. In the original STIM-2 data designation, anodic bias is established using a 32-bit command word as shown in Fig. 9. The desired 4-bit voltage level is latched by the clock strobe signal, and the DAC operates to set the anodic bias. This control logic has been designed and simulated to achieve the required performance. Capacitive DACs are well known to be more accurate than resistive DACs and can be lower in power; however, they also experience droop due to the leakage of charge from the storage nodes. This is of the order of 1mV/msec. Hence, they might be satisfactory

for the main current pulse DACs but would require periodic refreshing of the anodic bias level, which would need to remain set for some time during a typical experiment.

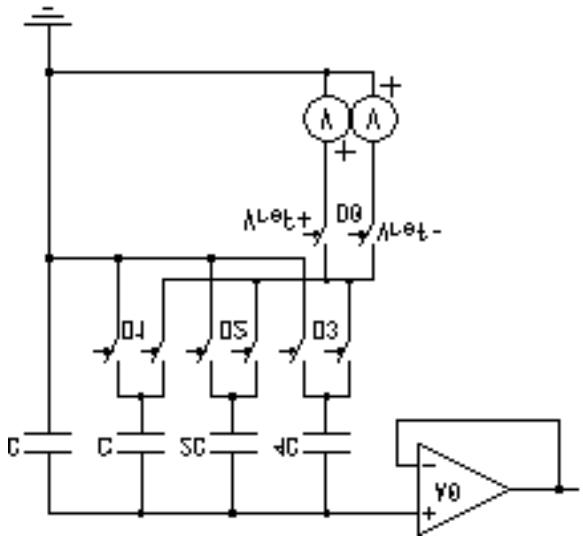

Fig. 6: Schematic of the capacitor-weighted voltage DAC

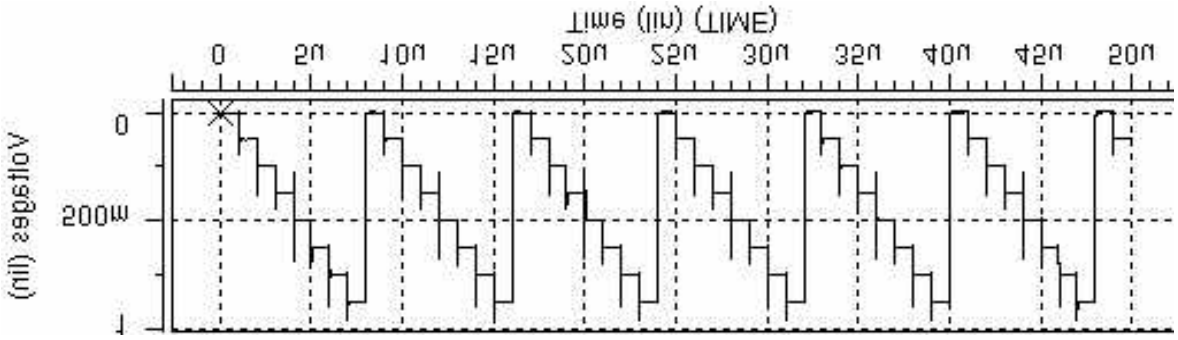

Fig. 7: Simulated outputs from 0 to 0.8V of the voltage DAC

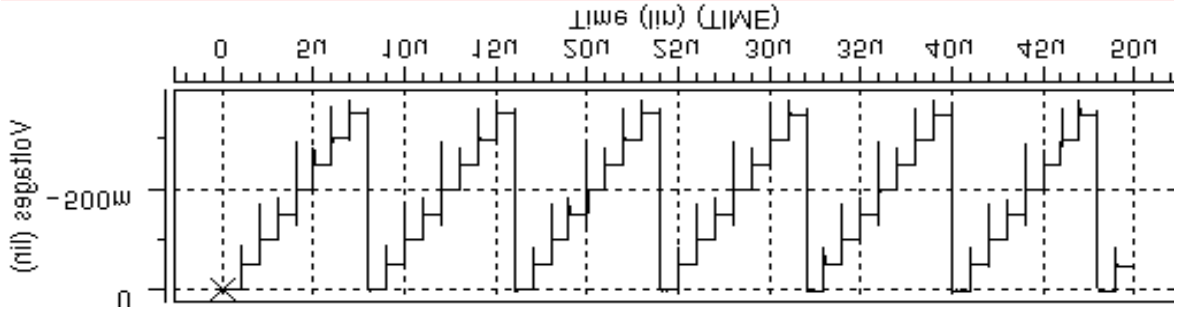

Fig. 8: Simulated outputs from -0.8 to 0V of the voltage DAC

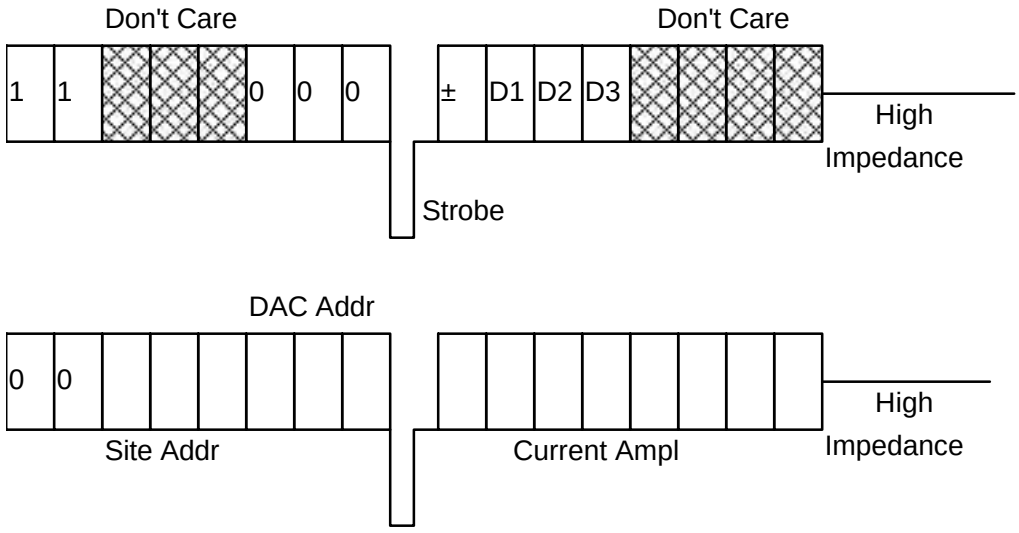

Fig. 9: Data designations for establishing the anodic bias level

Up to now, all the generations of stimulating probes have utilized dual ±5V supplies to obtain the required source and sink current operation. Some consideration has been given to the use of an alternative single supply to save power while possibly simplifying the design and process. For a single supply such as that used on the implantable microstimulator (FINESS) chips, charge balance is less of a problem since in one arrangement the same current sources can be used for sourcing and sinking. The currents are only steered between two different sites. The situation amounts to switching the ground (return) electrode. Figure 10 shows the schematic of an arrangement of two current sourcing DACs; operation is summarized in Fig. 11. The DACs set up sourcing currents that are available to the sites shown. If the left pull-down digital switch is closed and the right switch is open, then the right sourcing current flows from right to left through the sites, creating bipolar stimulation. If the left switch is open and the right switch is closed, bipolar stimulation is created in the opposite direction. The parallel RC circuit in Fig. 6 represents the impedance of the two sites in series. The source and sink currents are simulated in Fig. 12. The two currents are closely matched and no significant settling time is observed since only a single NMOS transistor is used as sink switch. The simulated linearity is also high as shown in Fig. 13. One important parameter of the DAC is its output saturation range in the face of double layer charging and the tissue spreading resistance (compliance voltage). Simulation shows (Fig. 14) that normal operation can be maintained up to at least 4.5V, which gives the DAC a wide output voltage capability.

Unfortunately, such current sources can only be used for bipolar stimulation unless a large-area reference electrode remote from the other sites is used as a return, and it must be switched to effectively source or sink current. Still more troublesome may be the fact that the scheme depends on the circuit ground (which receives current through the left and right NMOS pull-down switches) being isolated from the tissue. This is a

special concern since with active probes the p+ silicon substrate, which contains active junctions that operate under fixed reverse bias, must be at circuit ground. Although the silicon-tissue interface is much higher in impedance per unit area than the iridium oxide sites, the areas are vastly different. The importance of the conducting substrate in distorting current flow is not thought to be great, but in view of the complications a single-supply system may cause and the need for a second supply for closed-loop recording amplifiers, we plan to continue the use of a second supply. This causes no problems for wired probes, but somewhat complicates the telemetry interfaces. Some telemetry circuits can operate from a single supply in any case, however, and other circuits can be expanded from single-supply to dual-supply operation. Thus, we begin with single-supply designs, borrowing from past work as shown in the next section. We will also continue to explore the ramifications of single-supply operation to resolve remaining questions.

Fig. 10: Schematic of a simple single-supply current source

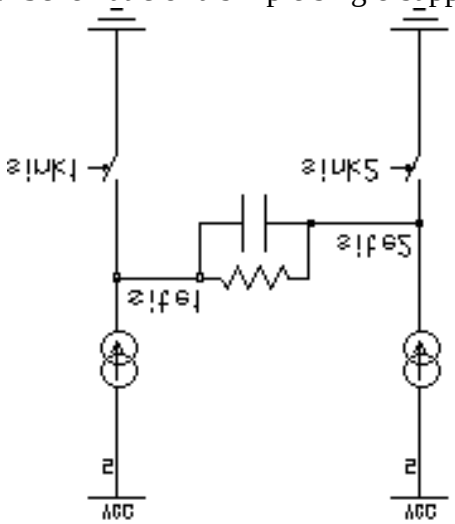

Fig. 11: Simple view of bipolar stimulation with single-supply current sources

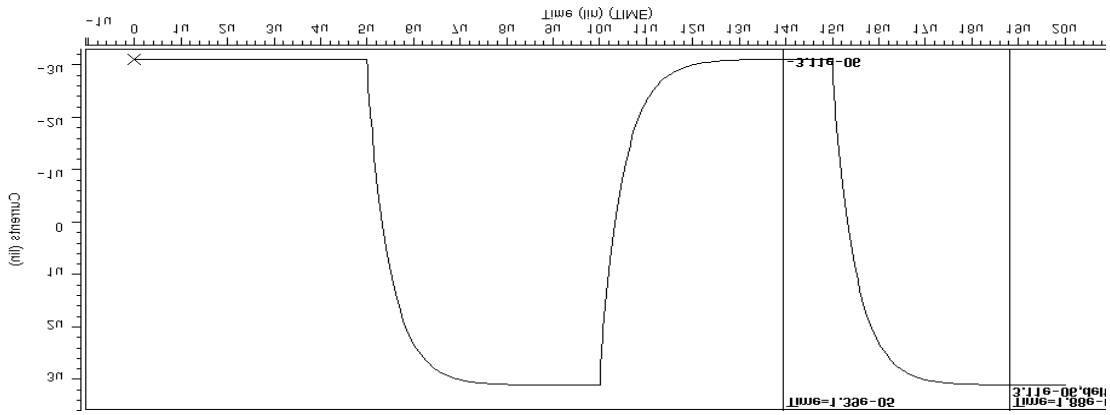

Fig. 12: Simulated source and sink currents from a single-supply current steering stimulus system.

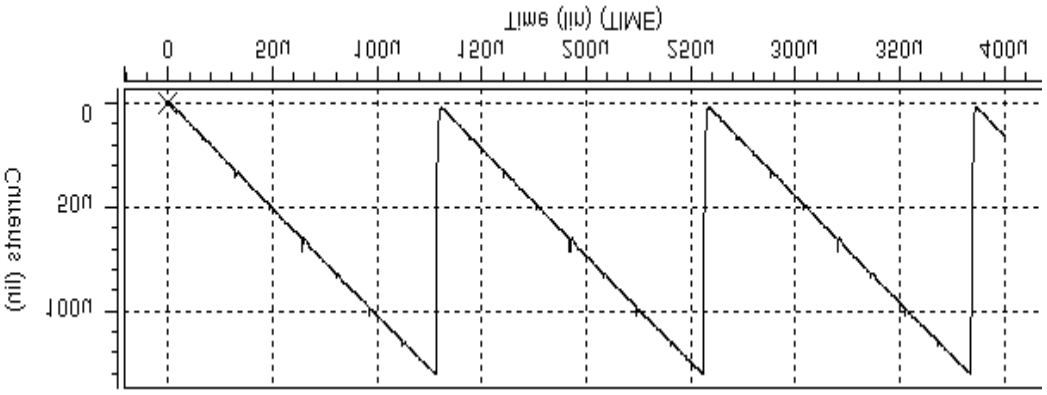

Fig. 13: Simulated linearity of a single-supply current source.

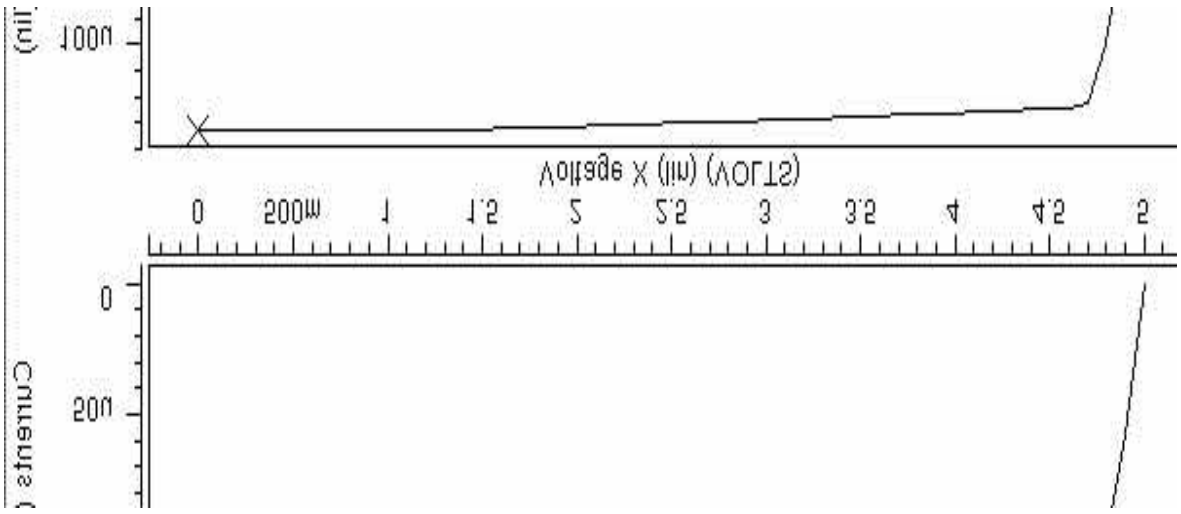

Fig. 14: Output current vs. output voltage for a single-supply source.

4. A Telemetry-Powered CNS Stimulating Microprobe

Present CNS stimulating probes (STIM-2, -2B/-3B) were not designed for use with telemetry but instead were hardwired to the outside world through a percutaneous plug. We have started work to develop a wireless platform-mounted probe interface to permit the percutaneous plug to be eliminated, providing rf power and input data to the implanted device and telemetering recorded signals to the outside world. During the past quarter, design of some of the individual circuit blocks needed to operate multi-channel stimulating probes using a telemetry link was started and completed. The circuit blocks needed are those for the power supply generator/regulator, clock recovery circuitry, and data detection. The design of these circuit blocks was based on similar blocks designed for implantable muscular stimulators, but with several modifications to improve performance or reduce power dissipation as needed. Since silicon probes utilize a BiCMOS process that incorporates a deep boron diffusion for defining the probe substrate, whereas FNS systems use a standard BiCMOS process without the boron diffusion, we have modified and compiled a new set of device and circuit parameters for use in the circuit simulator SPICE that are compatible with the probe process. This will allow complete flexibility in partitioning the system electronics between the probe and the platform in wireless stimulating systems. Using these new parameters, circuit blocks were designed, simulated and laid out. These circuit blocks are now in fabrication and it is expected that within the next three months they will be completed and ready for testing. In the following, a more detailed description of the individual circuit blocks is provided.

Voltage Regulator:

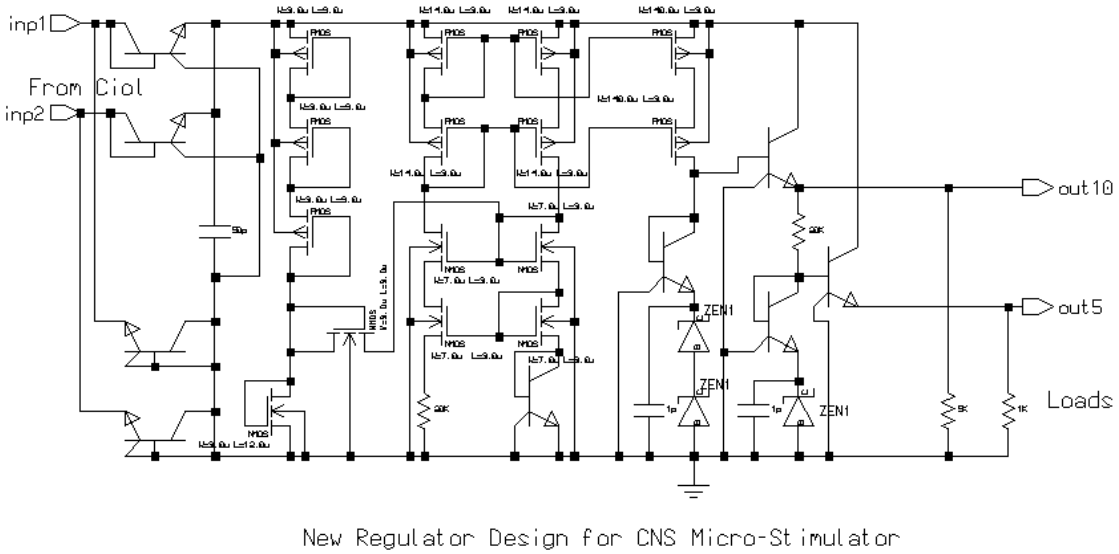

Fig. 15: Circuit diagram of the voltage regulator.

The voltage regulator circuit diagram is shown in Fig. 15. The regulator produces two output voltages, 10V and 5V, and its design is an improved version of the regulator circuit designed for the FINESS, a peripheral nerve stimulator. This regulator will be directly connected to the receiver coil through a full bridge rectifier. The rectifier capacitive filter is not very effective in eliminating output ripple because the capacitor should be integrated and cannot be more than tens of picofarads. To reduce the rectifier output ripple, a V_{be}-referenced current mirror is added that is highly supply-independent. The temperature dependence of the circuit is not a concern because it will be implanted and kept at 37°C. The current source generates a constant 35µA, a scaled version of which is forced through two 5.4V series Zener diodes to create a 10.8V reference voltage. This reference is then buffered to generate the regulated 10V output. This high level output is only used for stimulating pulses which should be capable of pushing current levels as high as 128µA into high-impedance stimulating sites. Other digital and analog blocks of the interface chip will be supplied by the 5V output to reduce the total power consumption.

Simulation results show that the new design has better load regulation and lower output ripple than its predecessor. The transient time simulation waveforms with 5K and 1K loads connected to 10V and 5V outputs, respectively, are shown in Fig. 16. For both outputs, supplying 20mW of power each, the output ripple is less than 8%. In Fig. 17, the input DC voltage sweep shows the regulator capability to restore the 10V output over a wide input voltage range from the coil. It also shows that the load regulation is better than 10% for loads higher than 2K (maximum of 50mW output power).

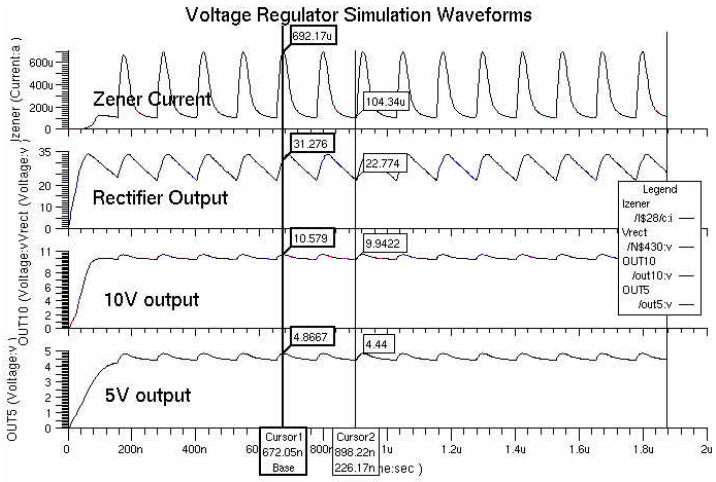

Fig. 16: Transient time simulation of the dual voltage regulator.

In addition to the dual voltage regulator, we have also designed and included a single 5V only regulator block on the chip for testing purposes. This circuit block is shown in Fig. 18 and is very similar to the design used for the dual voltage regulator. This regulator circuit can generate a 5V output with only an 8V input peak voltage.

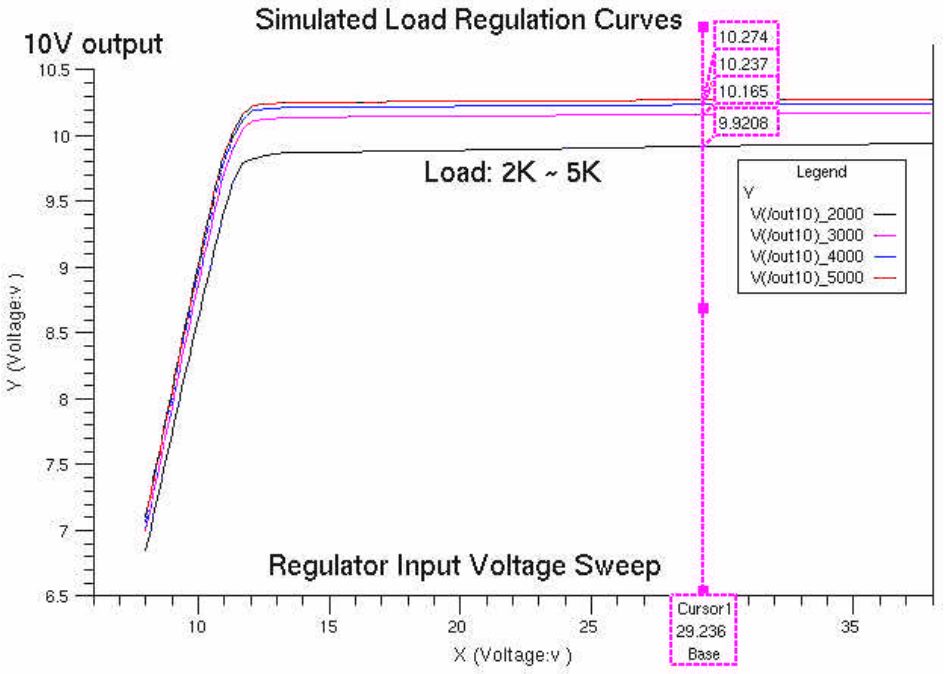

Fig. 17: The regulator DC input voltage sweep and load regulation.

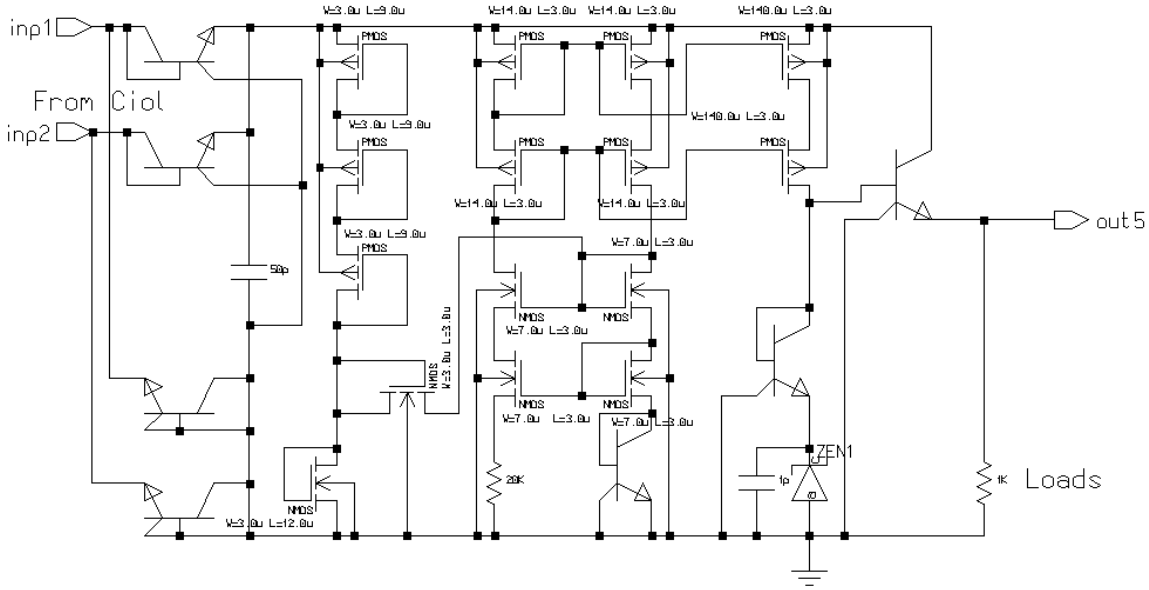

Fig. 18: 5V only regulator circuit diagram.

The dual voltage regulator layout is shown in Fig. 19. The size of the chip is 1.6mm by 0.84mm which is 20% less than the FINESS chip regulator area.

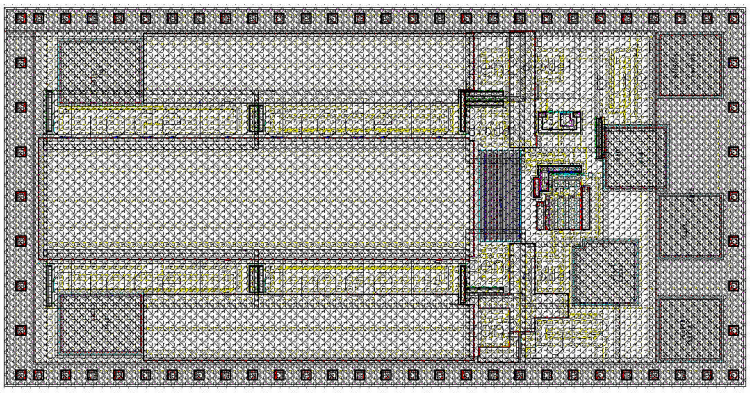

Fig. 19: Dual voltage regulator layout including input and output pads.

Power-On-Rest:

Figure 20 shows the circuit diagram of the power-on reset (POR) block needed to reset the entire system when it powers up. This mono-stable circuit guarantees the digital circuitry and registers always start from a known reset state when the implanted chip is powered up. This signal not only resets the interface chip internal circuitry but also resets all the connected micro-stimulating probes. A power-on-reset transient time simulation is shown in Fig. 21. A 10pF capacitor is linearly charged through a current source after applying power, decreasing the input voltage of a Schmitt trigger and finally changing its output state. The capacitor value, the current source amplitude and the Schmitt trigger switching levels are the parameters which control POR pulse width. For the values used in the above circuit, power-on delay is around 10µsec. This time should be adjusted to be longer than the power supply transient time.

Clock Recovery:

The clock recovery circuit is shown in Fig. 22. In this circuit a capacitive voltage divider synchronizes a ring oscillator with the half-rectified carrier signal. This circuit should be functional over a wide input range of received carrier amplitudes from 8V to 35V peak. A MOSFET current source discharges the capacitors after carrier reaches its peak, and a series BJT is added to protect it from input high voltage levels. The oscillator output is passed through more inverter stages to ensure a square-shaped clock signal output. Simulation waveforms are shown in Fig. 23. The component values are optimized through simulations for a 4MHz carrier input. Since the full-wave rectifier doubles the carrier frequency, a flip-flop is added to the output to generate the required 4MHz output. Another function of this flip-flop is to adjust the duty cycle of the clock signal to 50%.

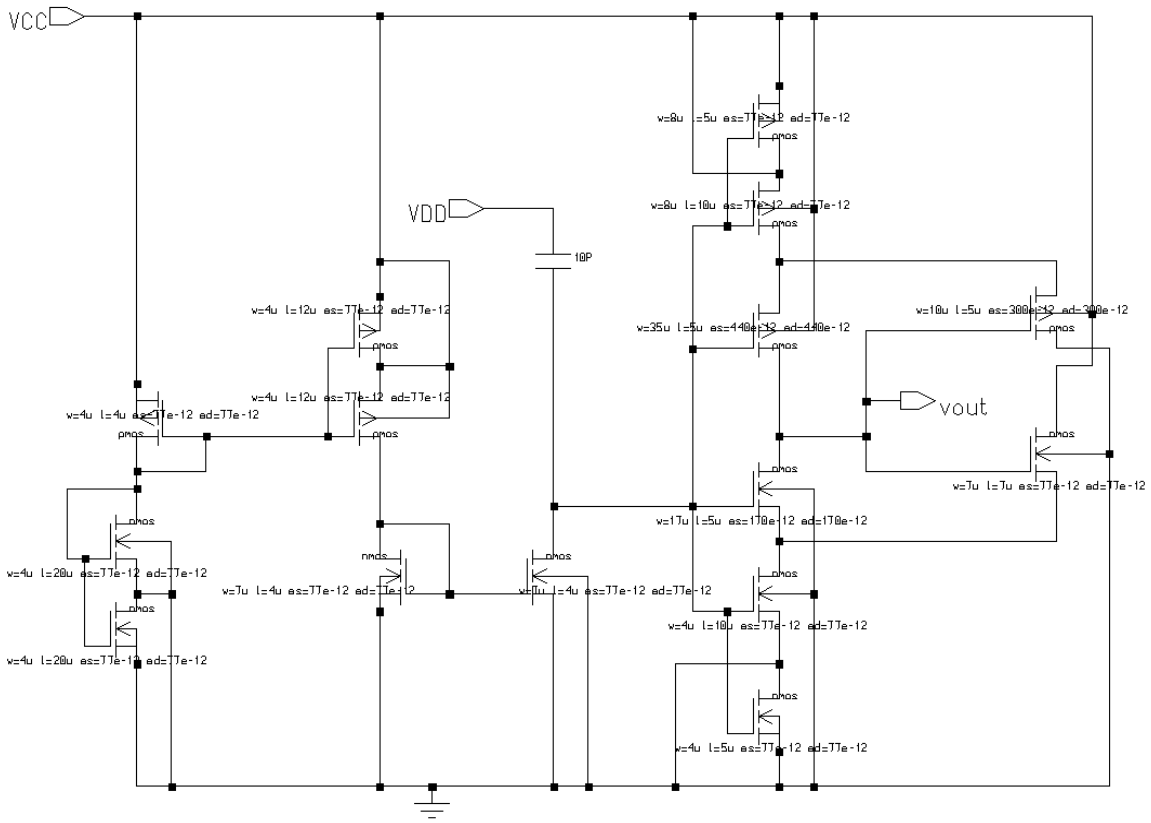

Fig. 20: Power-On-Reset circuit diagram.

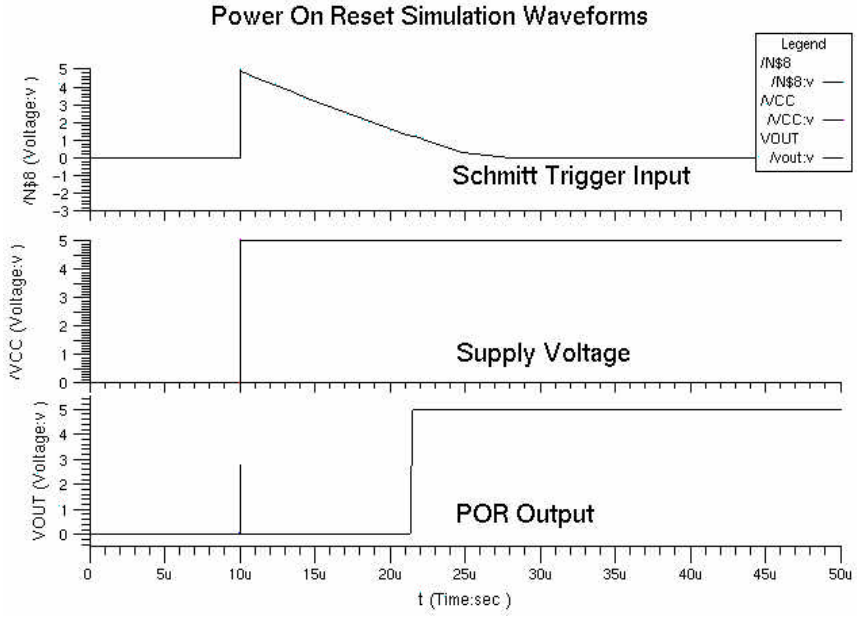

Fig. 21: Power-On-Reset transient time simulation waveforms.

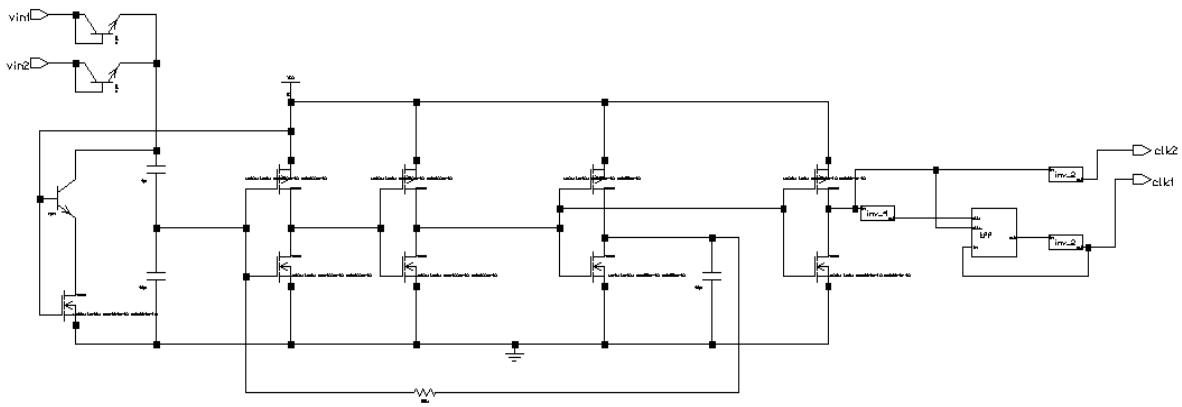

Fig. 22: Clock recovery circuit diagram.

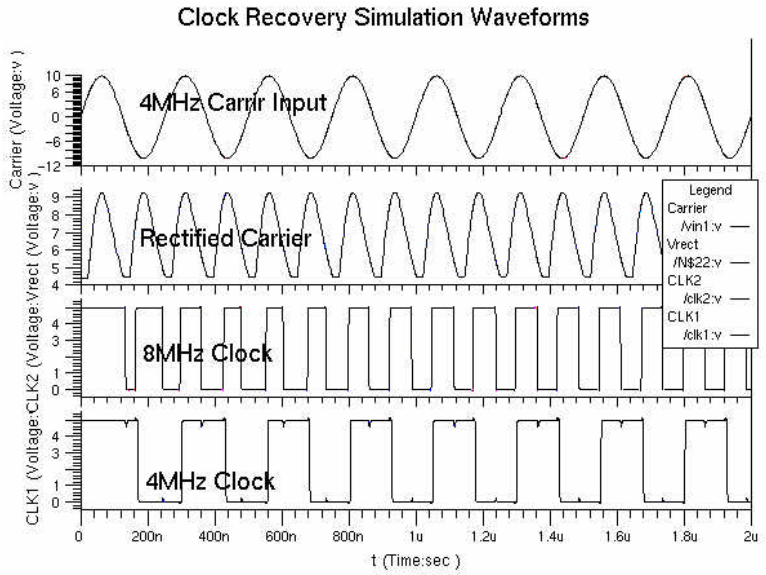

Fig. 23: Clock recovery transient time simulation waveforms.

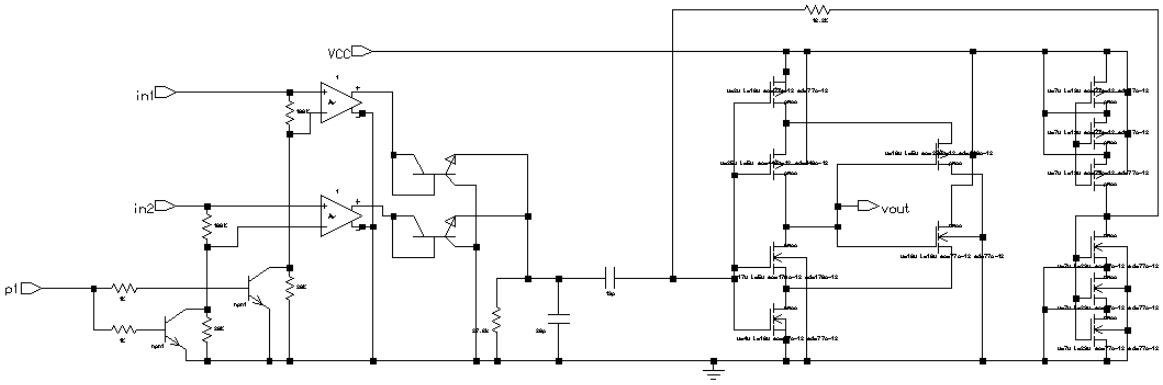

Fig. 24: Data detector circuit blocks.

Data Detector:

The data detector circuit is shown in Fig. 24. A combination of amplitude and pulse width modulation is used for data transfer in this telemetry system. The external transmitter system modulates the carrier amplitude based on the digital bit stream so that it is high in 66% and 33% of a bit period for low and high logic level bits, respectively. The amplitude-modulated rectified carrier is passed through a band-pass filter to remove the DC offset and the high-frequency carrier. Then a Schmitt trigger converts the analog signal to a PWM semi-digital bit stream. The switching levels of the Schmitt trigger stage should be chosen carefully based on the carrier modulation factor. To decrease the sensitivity of the circuit to the received signal modulation factor, an active load is added in parallel with the Schmitt trigger stage which adjusts the filtered signal base line. Data detector transient time simulation waveforms are shown in Fig. 25. The components added to the right of the rectifier in Fig. 24 are only for simulation purposes and are not present in the actual circuit.

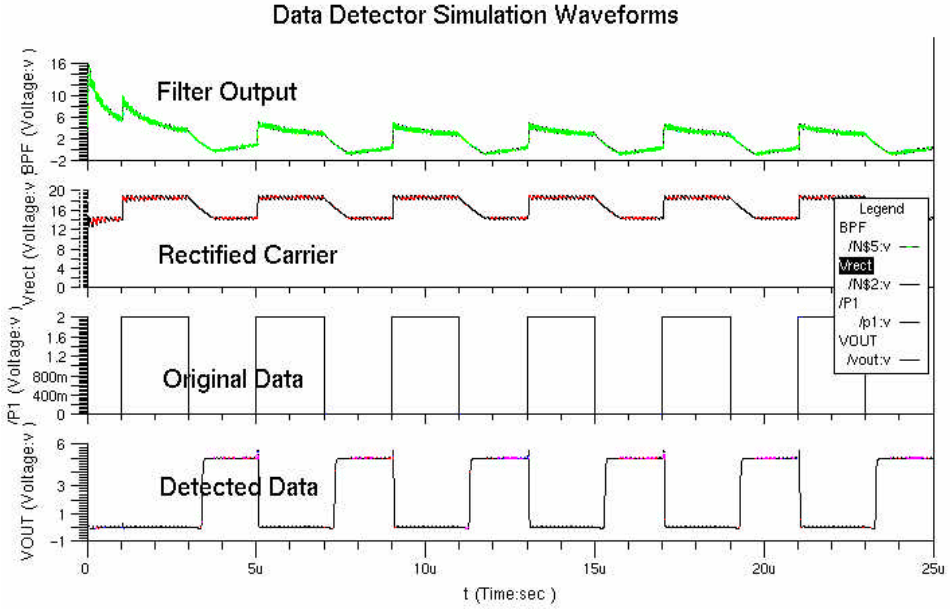

Fig. 25: Data detector transient time simulation waveforms.

The above circuit blocks have were laid out and included on a mask set of active microprobes (Fig. 26). They are currently in fabrication and should be available for testing in about in the next quarter.

In the next quarter, the other blocks of the wireless stimulating system will be designed and simulated and we will test the fabricated circuit blocks described above. Results from the these tests will be used to optimize and modify circuit designs that will be incorporated into a multi-channel stimulating probe with the rest of the circuitry needed for current delivery and control.

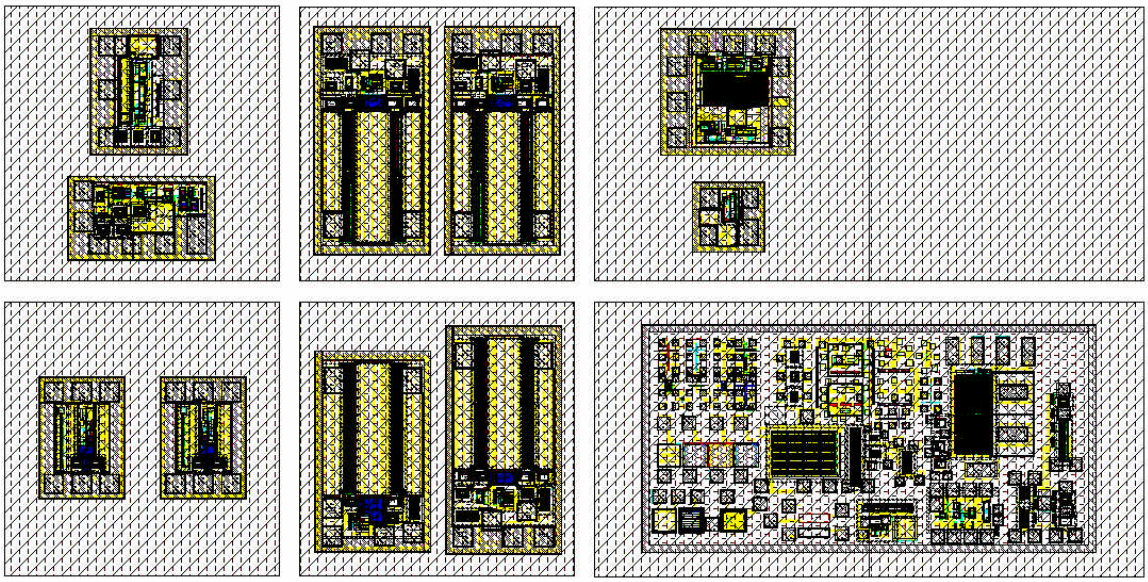

Fig. 26: Layouts of all the individual blocks on the mask set.

6. Conclusions

During the last quarter, the microassembly station used for the creation of multi-probe three-dimensional electrode arrays has been improved and used for the realization of a number of fully-functional units. The external electronics needed to interface with these arrays has been completed and is functional at frequencies of up to 9.5Mb/sec. Work has also gone forward on the redesign of STIM-2. Most of the redesigned probe has been completed, including a dedicated recording line and multi-level anodic bias option. A switched-capacitor digital-to-analog converter (DAC) has been explored for possible use in current generation, but in spite of advantages in power and accuracy is probably less attractive than the transistor/resistive DACs due to problems with leakage from the storage nodes and the problems of doing a high-quality sample-and-hold function on-chip. DAC circuits capable of operating from a single supply voltage have also been explored. These offer considerable circuit simplifications over dual-supply circuits but depend on electrical isolation between the probe and the tissue, which is not possible using active probes. The degree to which the conducting substrate may distort the current fields in such an arrangement is not precisely known but will be investigated. In the meantime, dual-supply operation will continue. Single- and dual supply circuits for a platform-mounted telemetry system have been designed and are now in fabrication. The circuits include voltage regulator, power-on reset, clock recovery, and data detector blocks. We expect to complete the design of STIM-2 during the coming term and to test the telemetry circuit blocks in preparation for a fully wireless active recording system.